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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/681,813   | 10/07/2003  | Alan Richard Ball    | ONS00524            | 6612             |
| 7590   | 04/22/2005  |                      | EXAMINER            |                  |
| James J. Stipanuk<br>Semiconductor Components Industries, L.L.C.<br>Patent Administration Dept - MD/A700<br>P.O. Box 62890<br>Phoenix, AZ 85082-2890 |             |                      | RILEY, SHAWN        |                  |
|  |             |                      | ART UNIT            | PAPER NUMBER     |
|  |             |                      | 2838                |                  |
| DATE MAILED: 04/22/2005  |             |                      |                     |                  |

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/681,813

Applicant(s)

BALL ET AL.

Examiner

Shawn Riley

Art Unit

2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9, 11-16 and 18-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9, 11-16 and 18-20 is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on oct 03 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

**DETAILED ACTION****Response to Applicants**

Applicants response has been carefully considered but not deemed persuasive. As per applicant's request further clarification as to requirement of labeling is found under 37 CFR 1.84(o) which 608.02 refers to. The whole point of the drawings is to not require a viewer to refer back to the spec to figure out things which can be made apparent by simply viewing labeling which results in a clear drawing(s).

Also, it is not clear why applicant has not also corrected the word "liner" in claims 6 and 7, they too remain objected to.

Applicants use the term "rectified sine wave having a non-zero period", this is repugnant to the use of the term 'rectified', applicants state it themselves, period refers to cyclic motion, a dc current is not cyclic and at best may be pulsed. When something is rectified it no longer has a period, especially something such as applicants full-wave rectifying invention. As long as applicants use a term such as a rectified signal having a period, this broadly recited 'limitation' is seen as being met by the prior art.

For at least the above reasons this action is made final.

***Drawings***

1. The drawing(s) is(are) objected to because they fail to label (figure(s) 1,3 and 4) what the element boxes 11, 81, 80, 60, 71, 19, and 22 are. Without some indication as to the content of the boxes (or preferably ansi symbols of the actual elements) it is not clear as to what

Art Unit: 2838

the elements are and they are not explanatory to a reader as a quick method of determining the general background of the invention.

See MPEP 608.02 and 37 CFR 1.84(o) -- **Legends**

Suitable descriptive legends may be used, or may be required by the Examiner, where necessary for understanding of the drawing, subject to approval by the Office. They should contain as few words as possible.

### ***Claim Objections***

1. Claims 6 & 7 are objected to under 37 C.F.R. 1.75(a) because of the following informalities: In claims 6 and 7, the term '*liner*' is taken to mean linear for examination purposes. Appropriate correction is required.
2. In claim 1, the term "*a non-zero period*" is not clear. A rectified signal does not have a period, it does not cycle and at best can only be a pulse, therefore for examination purposes a rectified signal will be taken as meaning a signal with a zero period. Appropriate correction is required.

***Claim Rejections - 35 U.S.C. § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-9, 11-12, 14-16, 18, and 20 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Perillo et al. (U.S. Patent 5,764,460).

As to claim 1;

A power supply control method comprising: coupling an input of a power supply system to receive an input voltage ( $V_{in}$  also represented as  $V_{ce}$ ) having a waveform of rectified sine wave having *a non-zero period* (this does not make sense a rectified signal does not have a period, it does not cycle and at best can only be a pulse, therefore for examination purposes a rectified signal will be taken as meaning a signal with a zero period) for each cycle of the waveform; coupling a load (connected to  $V_{out}$ ) to receive the input voltage; configuring a power supply controller (REG) to generate a load current through the load during a portion of a cycle of the input voltage when the input voltage ( $V_{ce}$ ) is between a first voltage ( $V_z$  see, e.g., column 5 lines 38- column 7 line 22) value and a second voltage value; (when the output voltage at  $V_{out}$  is higher than a

designated value, the comparator C1, comparing it to a predesignated voltage produced by CSVG, shuts off/disables the output load current, see, e.g., column 4 lines 49 through column 5 line 33) wherein the first voltage value and the second voltage value are less than a maximum value of the input voltage; and configuring the power supply controller to determine an average value of the load current, determine a difference between the average value of the load current and a desired average value and to use the difference and an instantaneous value of the load current to control the instantaneous value of the load current during the portion of the cycle to regulate the average value of the load current- over the period to the period average value of the load current (see, e.g., rejections in claims 7 and 8).

As to claim 2;

The method of claim 1 further including forming the power supply system to disable the load current when the input voltage is less than the first voltage (this occurs at the drop-out voltage, that is when the input voltage is too low for the regulator to function, see, e.g., column 7 lines 38-45).

As to claim 4;

The method claim 1 wherein configuring the power supply controller to generate the load current through the load during the portion of the cycle of the input voltage when the input voltage is between the first voltage value and the second voltage value includes forming the power supply controller to drive an output transistor (labeled as POWER) of the power supply controller in a linear mode

(the invention as described in the patent is a linear regulator) to generate the instantaneous current (definition of a linear regulator wherein the regulator will because of time delays, over/under – shoot a desired output value and thus reach a desired average current over a defined period of time).

As to claim 5;

The method of claim 4 further including forming the power supply controller to disable the load current when a voltage drop across the output transistor is a third voltage (the voltage across the transistor is taken by either C1 or the other comparator connected to Vbg) be taken as that is representative of the second voltage.

As to claim 6;

The method of claim 4 wherein forming the power supply controller to drive the output transistor of the power supply controller in the *liner* mode to generate the instantaneous current includes forming the power supply controller to generate an averaged signal that is representative of the average value of the load current over the cycle (see above discussion in claim 4).

As to claim 7;

The method of claim 6 wherein forming the power supply controller to drive the output transistor of the power supply controller in the *liner* mode to generate the instantaneous current includes forming the power supply controller to generate a deviation signal representative of a difference between the averaged signal (averaged signal between Ra and Rb) and a reference signal (Vbg), and to

generate an error signal representative of a difference between the deviation signal and the instantaneous current.

As to claim 8;

The method of claim 1 wherein configuring the power supply controller to generate the load current through the load during the portion of the cycle of the input voltage when the input voltage is between the first voltage value and the second voltage value; includes forming the power supply controller to generate the load current each cycle when the input voltage is greater than the first voltage value and less than the second voltage value (i.e., operate when the voltage is in a normal range as Perillo et al do).

***Claim Rejections - 35 U.S.C. § 103***

2. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this



Art Unit: 2838

section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

3. Claim 3 is rejected under 35 U.S.C. § 103 as being unpatentable over Perillo et al. (U.S. Patent 5,764,460). The Perillo et al. reference discloses the limitations of the invention as claimed as described above. However, Perillo et al. does not show a rectifier at the input source. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use utilize a rectifier at the input source since the examiner takes Official Notice of the equivalence of a rectified ac input and dc input from a dc source for their use in the regulating art and the selection of any of these known equivalents to a method of rectifying or providing a rectified input would be within the level of ordinary skill in the art.

***Allowable Subject Matter***

4. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and section 707.07(a) of the M.P.E.P. Claims 9, 11-16, and 18-20 are allowable.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

Art Unit: 2838

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

### *Conclusion*

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Mike Sherry who can be reached at 571.272.2084. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number 703.872.9306. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at <http://pair-direct.uspto.gov> wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

April 05



**Shawn Riley**  
**Primary Examiner**